Homework 1

(Due date: January 22nd @ 5:30 pm) Presentation and clarity are very important!

PROBLEM 1 (20 PTS)

- a) Simplify the following functions using ONLY Boolean Algebra Theorems. For each resulting simplified function, sketch the logic circuit using AND, OR, XOR, and NOT gates. (12 pts)
 - \checkmark $F = \overline{A(B + \overline{C}) + \overline{A}}$
 - \checkmark $F(X,Y,Z) = \prod (M_2, M_4, M_6, M_7)$

 $\checkmark \quad F = (Z + \overline{Y})(\overline{Z} + X)(\overline{Y} + X)$ $\checkmark \quad F = (\overline{X + Y})Z + \overline{X}YZ$

- b) For the following Truth table with two outputs: (8 pts)
 - Provide the Boolean functions using the Canonical Sum of Products (SOP), and Product of Sums (POS).
 - Express the Boolean functions using the minterms and maxterms representations.
 - Sketch the logic circuits as Canonical Sum of Products and Product of Sums.

x	У	z	\mathbf{f}_1	\mathbf{f}_2
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	1
1	1	1	0	1

PROBLEM 2 (20 PTS)

a) Complete the timing diagram of the logic circuit whose VHDL description is shown below: (5 pts)

```
library ieee;
use ieee.std logic 1164.all;
entity circ is
  port ( a, b, c: in std_logic;
                                            а
          f: out std logic);
end circ;
                                           b
architecture st of circ is
  signal x, y: std logic;
                                            С
begin
  x \leq a \text{ nor } b;
  y <= x xor c;
                                            f
  f \le y \text{ nand (not a)};
end st;
```

b) Complete the timing diagram of the following circuit: (5 pts)





c) The following is the timing diagram of a logic circuit with 3 inputs. Sketch the logic circuit that generates this waveform. Then, complete the VHDL code. (10 pts)



PROBLEM 3 (15 PTS)

Design a circuit (<u>simplify your circuit</u>) that verifies the logical operation of a 3-input XNOR gate. f = '1' (LED ON) if the XNOR gate does NOT work properly. Assumption: when the XNOR gate is not working, it generates 1's instead of 0's and vice versa.



PROBLEM 4 (30 PTS)

A 16-letter keypad produces a 4-bit code as shown in the table. We want to design a logic circuit that converts those 4-bit codes to Braille code, where the 6 dots are represented by LEDs. A raised (or embossed) dot is represented by an LED ON (logic value of `1'). A missing dot is represented by a LED off (logic value of `0').

- ✓ Complete the truth table for each output (Q_0 - Q_5).
- \checkmark Provide the simplified expression for each output (Q₀-Q₅). Use Karnaugh maps for Q₅-Q₂ and the Quine-McCluskey algorithm for Q₁-Q₀. Note it is safe to assume that the codes 1110 and 1111 will not be produced by the keypad.



PROBLEM 5 (15 PTS)

The following die has a sensor on each side. Whenever a side rests on a surface, the sensor on that side outputs a logic '1' (which is transmitted wirelessly to a controller); otherwise, it outputs a '0'. The sensors are named s_i , where i is the number printed on the respective side.

We want to design a circuit that reads the state of the 6 sensors and outputs the value of the upper surface. That decimal value is represented using the binary number system (see table below). A LED ON is represented by the logic value of '0', and a LED OFF is represented by a logic value of '1'.

For example, in the figure below, the resting side has six dots while the upper surface has one. The resulting decimal number is then 1', which is represented by 001 on the LEDs. The state of the sensors is S6=1, S5=0, S4=0, S3=0, S2=0, S1=0.

Under normal circumstances, we expect only one sensor activated at a time. However, due to a variety of problems, we might have the following cases:

- Two or more sensors produce a '1' at the same time: In this case, the state of the LEDs must be 000.
- No sensor produces a '1': In this case, the state of the LEDs must be 000.
- ✓ Using the state of the sensors as inputs, provide the Boolean expression for each LED: L₂, L₁, L₀. Use the canonical Sum of Products for each function.

